## Review Article

# A study of converter configurations for vehicular applications 

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#### Abstract

Renewable energy sources like hydro, wind, geothermal and solar along with fuel cells are nowadays solutions to the global energy crisis, environmental issues, and fossil fuel exploitation. The nature of the output of these renewable sources is D.C. The role of DC-DC converters in the integration of energy sources with microgrids is vital. These converters find their major applications in power generation, energy systems, vehicular applications, portable electronic devices, aerospace, etc. These converters help to boost the voltage and improve the reliability, stability, efficiency, and performance of the system. This study gives a brief overview of three DC-DC converters of non-isolated topology. They are: Clamped H-type boost DC-DC converter, Multi-Port Dual-Active-Bridge DC-DC Converter, and Four-Phase Interleaved FourSwitch Buck-Boost Converter. This study will make researchers learn and make their concept clear about the operation, performance, and usage of these converters.


## Introduction

The rising concern of pollution and energy shortage has led human society to shift towards clean and sustainable energy sources. Integration of renewable energy sources like solar, wind, hydro, etc. into microgrids has opened ways for mitigating growing energy demand [1,2]. The output of these sources are D.C supply. Electric Vehicles (EV) and Fuel Cell Electric Vehicles (FCEV) are substitutes for conventional vehicles. These vehicles use electric motors in place of IC engines [3,4]. The power electronic converters act as the intermediaries between power generation and load. They have replaced conventional voltage divider circuits, power conversion circuits, and rheostats which have low efficiency and low output voltage [5,6]. The DC-DC converters were first introduced in the year 1920. They have a wide area of application. Converters stabilize the output voltage of the system during intermittent conditions. The quality of power obtained from renewable energy systems depends heavily on the control technique and stable operation
of the power converter [7-9]. Boost converters were the first converters used; all converters are derived from this. Boost converters are more widely and popularly used when it comes to renewable energy applications as they are simple in design [10]. Theoretically, the voltage gain in the case of a boost converter can go to infinity for unity as the duty cycle. But, with an increase in duty cycle, there are certain issues like shorter turn-off period of a switch, increased conduction losses, current ripples, turn-off current, and high voltage stress which makes the cost of high voltage stress switch more [11].

To improve the reliability of the system and to achieve a constant output voltage at the load side, a wide voltage gain DC-DC converter is used to connect with a high-voltage DC bus [12,13]. The DC-DC converters used for this purpose should have some specific features like high efficiency, high reliability, and small size [14]. The selection of a proper DC-DC converter for the desired application is a very crucial step as it affects the
system's output and operating performance largely. In the case of FCEVs, the converter used must have a continuous input current and low current ripple [15]. The DC-DC converters in the literature are classified based on isolated and nonisolated topologies for obtaining wide voltage gain. An isolated DC-DC converter has a high-frequency transformer located between the input and output side to provide galvanic isolation [16] to protect sensitive loads by enhancing safety and also transmitting the input power to the output side. The output in these converters has a high immunity to noise interference. They are more suitable for applications where a high voltage gain ratio is required due to a magnetic transformer. This makes the converter bulky and complex. In the case of twostage power transformation, the two stages are DC-AC-DC [17]. The non-isolated DC-DC converters are cost-effective, simple in design, and do not have galvanic isolation. Researches are carried out on non-isolated converters for improved switching, enhanced efficiency, fault-tolerant operation, control and switching strategies, and renewable energy applications [1820]. The non-isolated type of DC-DC converters due to their high efficiency and low cost are used in FCEVs. Figure 1 shows different types of converters.

The non-isolated converters of high voltage gain mainly focus on multistage techniques, switched capacitors, voltage multipliers, switched inductors, and coupled inductors [21,22]. It is easy to achieve high voltage gain in a coupled inductor converter but a large current ripple is seen in the case of a singlestage single-phase-coupled inductor converter which reduces the life span of FCs in FCEV [23]. A switched inductor converter attains high voltage gain but it exerts a high voltage stress on diodes [24]. A boost-type DC-DC converter can provide a wide voltage range when used with a switched capacitor structure [25]. A three-level DC-DC boost converter having low input current ripple and limited voltage gain for interfacing fuel cell stack is presented in [26]. A high-frequency Pulse Width Modulation (PWM) voltage is applied between the grounds
of the input and output port which causes Electromagnetic Interference (EMI) problems and maintenance issues. A common ground structure to increase the reliability of the converter is presented in [27]. A converter having a wide input voltage range, lower voltage gain, low input current ripple, and non-common ground topology is presented in [28]. A larger duty cycle enhances the voltage gain but it also increases the conduction loss in power switches. A switched capacitor-based double switch boost converter with a non-common ground topology of duty cycle in the range $0-0.5$ to reduce conduction loss of power switch is proposed in [29]. This study gives an overview of three such converters namely a Clamped H-type boost DC-DC converter With a Wide Voltage-Gain Range, a Multi-Port Dual-Active-Bridge DC-DC Converter, and a FourPhase Interleaved Four-Switch Buck-Boost Converter. The converters are explained in sections II, III, and IV respectively. The study is concluded in section $V$.

## Clamped H-type boost DC-DC converter

The clamped H-type boost DC-DC converter is interfaced with the FC stack in FCEVs where it works as a step-up device. The output voltage of FC stacks is DC in nature and of low value which cannot be used directly and is thus boosted and regulated using a step-up stage. This converter has various advantages such as a wide input voltage range, high voltage gain, minimum conduction losses, reduced input current ripple, and voltage stress on capacitors and power semiconductors. This increases the efficiency and reliability of the converter making it capable of use in FCEV. The authors in [30] used this converter along with a switched capacitor structure. The capacitor-clamped $H$-type structure consists of two switches $S_{1}, S_{2}$ along with $\mathrm{Q}_{1}$, $\mathrm{Q}_{2}$, diodes $\mathrm{D}_{1}$, and $\mathrm{D}_{2}$, capacitor $\mathrm{C}_{1}$, and inductor L . The structure of the switched capacitor consists of diodes $\mathrm{D}_{3}, \mathrm{D}_{4}$, and $\mathrm{D}_{5}$ and capacitors $\mathrm{C}_{2}, \mathrm{C}_{3}$, and $\mathrm{C}_{4}$. The advantages of the inclusion of a switched capacitor structure are a reduction in voltage stress from semiconductors and capacitors and high voltage gain. A


Switched-capacitor-based DC-DC converter was proposed in [31] with one capacitor and one diode less than this converter and a higher voltage gain. A non-common ground of inputoutput, large input current ripple, and one diode with high voltage stress were some of its disadvantages. The analysis of the clamped converter is done during the continuous conduction of the input current. The duty cycle of $Q_{1}$ is $d_{1}$ and $Q_{2}$ is $d_{2}$ where $d_{1}=d_{2}=d$ with $180^{\circ}$ phase difference between the two gates signals [30]. The operating condition of $\mathrm{Q}_{4}$ and $\mathrm{Q}_{2}$ decides the number of switching states. A total of four switching states for operation are there. They are $00,01,10$, and 11 . The value ' 0 ' represents the OFF state and ' 1 ' represents the ON state of the power switches. The switching state 11 is achieved only when the value of duty cycle $d$ is higher than 0.5 . During the range of the duty cycle between $0.5-1$, the switching states are 01,10 \& 11 which means at least one switch among $Q_{1}$ and $Q_{2}$ has to be in the ON state, leading to continuous charging of the inductor. Due to this, the range of the converter's duty cycle lies between 0 to 0.5 .

The sequence of three switching states of the converter during each switching period is $10-00-01-00$. During $\mathrm{S}_{1} \mathrm{~S}_{2}$ $=10$ as depicted in Figure 2(a), the switch $\mathrm{Q}_{1}$ is $O N$ and $\mathrm{Q}_{2}$ is in OFF condition. The polarization of diodes $D_{1}$, and $D_{4}$ is inverse whereas for diodes $D_{2}, D_{3} \& D_{5}$ it is direct. The charging of inductor L is accomplished through a rising current $\mathrm{i}_{\text {in }}$ linear in nature. A parallel connection could be observed between capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{4}$ as well as between $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$. Further, a series of connections of these elements is done to supply power to the load. $\mathrm{S}_{1} \mathrm{~S}_{2}=00$ indicates the OFF state of switches $\mathrm{Q}_{4}$ and $\mathrm{Q}_{2}$ as shown in Figure 2(b). In this case, a direct polarization of diodes $D_{1}, D_{2}, D_{3}$, and $D_{5}$ is observed whereas inverse polarization of diode $\mathrm{D}_{4}$ is done. A linear decrement in the inductor current could be observed. The energy of inductor L is transferred to $\mathrm{C}_{1}$ and $\mathrm{C}_{4}$. Inductors L and $\mathrm{C}_{2}$ not only charge the capacitor $\mathrm{C}_{3}$ but also supply the load. The switch $\mathrm{Q}_{4}$ is in OFF condition whereas $\mathrm{Q}_{2}$ is in ON condition during $\mathrm{S}_{1} \mathrm{~S}_{2}=01$. This is shown in Figure 2(c). Here, $D_{1}$ and $D_{4}$ are directly polarized whereas the diodes $\mathrm{D}_{2}, \mathrm{D}_{3}$, and $\mathrm{D}_{5}$ have inverse polarization. The inductor $L$ gets charged through the current $i_{i n}$ that has a linear
incremental nature. A parasitic resistance limits the current of diode $\mathrm{D}_{4}$ of the converter. Capacitor $\mathrm{C}_{4}$ charges $\mathrm{C}_{2}$ whereas $\mathrm{C}_{3}$ supplies the load. Figure 2(d) represents an equivalent circuit of the converter.

This converter offers a wide input voltage range along with high voltage gain. The verification of these converters is possible for all ideal components. The values of inductances and capacitances are considered to be large enough with constant voltages appearing across the capacitors. The diodes $D_{1}$ and $D_{5}$ are forward-biased. The voltages across $C_{1}$ and $C_{4}$ are equal as they are connected in parallel same is the case with capacitance $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$. The expression of the voltage gain of this converter while operating in continuous current mode can be deduced using volt second balance of the inductor:

$$
\left\{\begin{array}{c}
2 V_{\text {in }} d+\left(V_{\text {in }}-V_{1}\right)(1-2 d)=0  \tag{1}\\
V_{1}=V_{2}=V_{3}=V_{4} \\
V_{0}=V_{3}+V_{4}
\end{array}\right\}
$$

Where, $V_{\text {in }}$ represents input voltage, $V_{0}$ represents output voltage, $V_{1}, V_{2}, V_{3}, V_{4}$ represents the voltage across the capacitors namely $\mathrm{C}_{1}, \mathrm{C}_{2}, \mathrm{C}_{3}$ and $\mathrm{C}_{4}$. Eqn. (1) could be rewritten as:

$$
\begin{align*}
& V_{0}=\frac{2}{1-2 d} V_{i \mathrm{n}}  \tag{2}\\
& V_{1}=V_{2}=V_{3}=V_{4}=\frac{1}{1-2 d} V_{i \mathrm{n}} \tag{3}
\end{align*}
$$

On the basis of eqn. (2) and eqn. (3), the voltage gain can be determined by:

$$
\begin{equation*}
M=\frac{2}{1-2 d} \tag{4}
\end{equation*}
$$

Where d is the duty factor of range $o<d<0.5$. The range of $d$ is so selected to avoid a narrow pulse of waveforms of PWM voltage. To avoid a narrow pulse of waveforms of PWM voltage all power semiconductor components, during the high


Figure 2: Configuration of Clamped H-type boost DC-DC converter. Different switching states of the converter are shown in Figure 2(a), Figure 2(b) \& Figure 2(c). The equivalent circuit of this converter is represented in Figure 2(d).


Figure 2(a): At first switching state.


Figure 2(b): At second switching state.


Figure 2(c): At third switching state.


Figure 2(d): Equivalent circuit of clamped H-type boost converter in switching state.
voltage gain are kept at ON state time whereas a time period close to 0.5 T is chosen for OFF state time during each cycle. The converter achieves high voltage gain for a small value of duty cycle d i.e. 0.5 which further helps in decreasing conduction loss of power switches. The converter experiences a decrease in conduction loss for a short conduction time of the switch with voltage gain lying between 2 and 20 . The voltage gain $M$ and the overall conduction time $t_{\text {on }}$ of the switch can be related using the following expression:

$$
\begin{equation*}
t_{\text {on }} \frac{M-2}{M} \times T \tag{5}
\end{equation*}
$$

The value of the average inductor current $I_{L}$ can be found out by:

$$
\begin{equation*}
I_{L}=\frac{2}{1-2 d} \times \frac{V_{o}}{R} \tag{6}
\end{equation*}
$$

Here, $R$ represents the load resistor. During $\mathrm{S}_{1} \mathrm{~S}_{2}=10$, a linear increment of inductor current occurs which can be given by

$$
\begin{equation*}
\Delta i_{L}=\frac{d \times V_{i \mathrm{n}}}{L f} \tag{7}
\end{equation*}
$$

The inductor ripple current is denoted by $i_{L}$ and switching frequency is denoted by $f$. The value of the current ripple ratio $r$ for an inductor can be determined by using eqn. (6) and eqn. (7):

$$
\begin{equation*}
r=\frac{\Delta i}{I_{L}} \frac{d(1-2 d)^{2} \times R}{4 L f} \tag{8}
\end{equation*}
$$

In real time, the value of $M$ is kept between 5 and 16 . For $M$ greater than 5, there is a decrement in the ripple ratio of the input current of this converter leading to a continuous waveform of input current. The value of $r$ is $28.5 \%$ when the voltage gain reaches 16 .

Since, $\mathrm{D}_{1}$ and $\mathrm{C}_{1}, \mathrm{Q}_{2}$ and $\mathrm{C}_{1}$, and $\mathrm{D}_{4}$ and $\mathrm{C}_{2}$ are in a parallel state when $Q_{2}, D_{1}$, and $D_{4}$ are in an OFF state whereas $Q_{1}, D_{2}$, and $\mathrm{D}_{3}$ are in ON states, the voltage across the parallel-connected power semiconductors will be equal. The voltage across these components is shown in eqn. (9)

$$
\left\{\begin{array}{c}
V_{Q 2}=V_{D 1}=V_{C 1}=\frac{1}{2} V_{o}  \tag{9}\\
V_{D 3}=V_{D 4}=V_{C 2}=\frac{1}{2} V_{o} \\
V_{Q 1}=V_{D 2}=V_{C 1}=\frac{1}{2} V_{o} \\
V_{D 5}=V_{D 3}=\frac{1}{2} V_{o}
\end{array}\right\}
$$

This shows that in this converter the voltage stress across all capacitors and power semiconductors is half of the output voltage. This converter also possesses a frequency doubling characteristic which leads to a reduction of the volume of the capacitor and inductor used here. The major limitation of this converter is its usage of five diodes which increases the reverse
recovery losses and conduction losses which further decreases the efficiency of this converter. However, the power switches of this converter have small conduction losses. The waveform of this converter is shown in Figure 3.

## Current-fed hybrid dual active bridge DC-DC converter

The converter consists of four power MOSFETS $S_{1}, S_{2}, S_{3}$, and $\mathrm{S}_{4}$ at the input side operating as a dual boost half-bridge converter along with two inductors $L_{1}$ and $L_{2}$. The output side consists of an auxiliary half-bridge and a full bridge [32]. A similar current-fed DC/DC converter is proposed in [33] based on the FC model and load disturbance conditions. The auxiliary half bridge is constructed using $\mathrm{S}_{9}$ and $\mathrm{S}_{10}$ MOSFETS whereas the full bridge is constructed of four MOSFETS namely $\mathrm{S}_{5}, \mathrm{~S}_{6}$, $\mathrm{S}_{7}$, and $\mathrm{S}_{8}$. A high-frequency transformer with a turn ratio of 1 : n connects the two sides. The transformer's leakage inductance is represented by L. Figure 4 represents this converter. The converter has a voltage conversion ratio that is given by:

$$
\begin{equation*}
M=\frac{V_{0}}{2 n V_{i n}} \tag{10}
\end{equation*}
$$

At the input side, the switches $\mathrm{S}_{1}$ and $\mathrm{S}_{2}, \mathrm{~S}_{3}$ and $\mathrm{S}_{4}$ are operated complimentarily with a fixed duty cycle of $50 \%$. The switches $\mathrm{S}_{2}$ and $\mathrm{S}_{4}$ are separated by a phase shift of $\mathrm{T}_{5} / 2$. The switching period is denoted by $\mathrm{T}_{\mathrm{s}}$. On the output side, switches $\mathrm{S}_{5}$ and $\mathrm{S}_{6}$, $S_{7}$ and $S_{9}$, and $S_{8}$ and $S_{10}$ are also complement to each other. $S_{5}$ and $S_{6}$ have a fixed duty cycle of $50 \%$ whereas the gating signal of power switch $S_{5}$ lags behind $S_{1}$ by a phase shift ratio of $\phi$. The power switches $S_{7}$ and $S_{8}$ are turned on along with $S_{5}$ and $S_{6}$. The Zero-Voltage Switching (ZVS) for a wide operating range can be obtained for all switches for an appropriate duty cycle. $i_{L}$ denotes the current flowing through the leakage inductor. The voltage across points $1 \& 2$ is represented by $V_{12}$ whereas $V_{34}$ represents the voltage across points $3 \& 4$.

The operation of the entire switching period of this converter could be separated into 12 stages but due to symmetry in the operating mode, the half-switching cycle will be discussed


Figure 3: Waveforms of Clamped H-type boost DC-DC converter.
since the other half is similar to it. The configurations of the converter at different durations of the switching periods from $t_{1}-t_{7}$ are shown in Figure $4(a-f)$ respectively. Before $t_{1}$, the power switches $\mathrm{S}_{1}, \mathrm{~S}_{3}, \mathrm{~S}_{7}, \mathrm{~S}_{9}, \mathrm{~S}_{10}$ are on and $\mathrm{i}_{\mathrm{L}}$ decreases linearly. At the instant $\mathrm{t}_{1}, \mathrm{~S}_{1}$, and $\mathrm{S}_{3}$ are turned off. This makes the junction capacitors attached to the switches at the input side resonate with $\mathrm{L}, \mathrm{L}_{1}$, and $\mathrm{L}_{2}$. The difference between the currents $i_{L 1}$ and $i_{L}$ charges the capacitor of $\mathrm{S}_{2}$ and discharges the capacitor of $S_{1}$ until the voltage across the drain to the source of
$\mathrm{S}_{1}$ reaches zero. After that, the diode of $\mathrm{S}_{1}$ will start conduction after the gating signal of $\mathrm{S}_{1}$. Similarly, the sum of $\mathrm{i}_{\mathrm{L}}$ and $\mathrm{I}_{\mathrm{L} 2}$ will charge the capacitor of $\mathrm{S}_{3}$ and discharge the capacitor of $\mathrm{S}_{4}$ until ZVS is obtained. At instant $\mathrm{t}_{2}, \mathrm{~S}_{1}$, and $\mathrm{S}_{4}$ are turned ON. The ZVS can be obtained if $\mathrm{L}, \mathrm{L}_{1,}$ and $\mathrm{L}_{2}$ are properly designed. After the completion of the resonance period, $\mathrm{V}_{12}$ is equal to $\mathrm{V}_{\mathrm{c}}$ and $\mathrm{V}_{34}$ is equal to $-V_{0} / 2$ which results in a linear increment of $I_{L}$. At this time, the voltage across both $\mathrm{S}_{7}$ and $\mathrm{S}_{8}$ is $\mathrm{V}_{0} / 2$. This can be represented by the following equation:


Figure 4: Schematic diagram of the current-fed hybrid dual active bridge (DAB) DC-DC converter. The configurations of the converter at different switching periods are shown in Figure 4(a-f).


Figure 4(a): Operating period $\mathrm{t}_{1}-\mathrm{t}_{2}$.


Figure 4(b): Operating period $\mathrm{t}_{2}-\mathrm{t}_{3}$.


Figure 4(c): Operating period $\mathrm{t}_{3}-\mathrm{t}_{4}$.


Figure 4(d): Operating period $\mathrm{t}_{4}-\mathrm{t}_{5}$.


Figure 4(e): Operating period $\mathrm{t}_{5}-\mathrm{t}_{6}$.


Figure 4(f): Operating period $\mathrm{t}_{6}-\mathrm{t}_{7}$.

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$$
\left\{\begin{array}{c}
V_{12}=V_{c}  \tag{11}\\
V_{34}=-V_{o} / 2 \\
i_{L}(t)=i_{L}\left(t_{2}\right) \frac{V_{12}-V_{34} / n}{L}\left(t-t_{2}\right)
\end{array}\right\}
$$

$\mathrm{S}_{6}$ and $\mathrm{S}_{10}$ are turned off at $\mathrm{t}_{3}$. The junction capacitors of $\mathrm{S}_{6}$, $\mathrm{S}_{7}$ and $\mathrm{S}_{10}$ will get charged whereas junction capacitors of $\mathrm{S}_{5}$ and $\mathrm{S}_{8}$ will discharge due to secondary current $\mathrm{i}_{2}$ of the transformer till voltage across $\mathrm{S}_{5}$ and $\mathrm{S}_{8}$ reaches zero. The voltage across $\mathrm{S}_{6}$ and $\mathrm{S}_{7}$ increases to $\mathrm{V}_{0}$ whereas across $\mathrm{S}_{10}$ the voltage increases to $\mathrm{V}_{0} / 2$. This results in the conduction of body diodes of $\mathrm{S}_{5}$ and $\mathrm{S}_{8}$ until their gate signals arrive. At time instant $\mathrm{t}_{4}$, the power switches $\mathrm{S}_{5}$ and $\mathrm{S}_{8}$ are turned on with the ability of ZVS . The value of $\mathrm{V}_{\mathrm{c}}$ is less than $\mathrm{V}_{0} / n$, which will result in a linear decrease of current $\mathrm{I}_{\mathrm{L}}$ as per the relationship given in eqn. (12). At this condition, there will be no flow of secondary current $i_{2}$ through the bidirectional switch constructed by $\mathrm{S}_{9}$ and $\mathrm{S}_{10}$. At $\mathrm{t}_{5}$, the switch $\mathrm{S}_{8}$ is turned off. The junction capacitors of $\mathrm{S}_{8}$ will be charged whereas that of $\mathrm{S}_{7}$ and $\mathrm{S}_{10}$ will be discharged due to $\mathrm{i}_{2}$ till the $\mathrm{V}_{\mathrm{DS}}$ voltage of $\mathrm{S}_{8}$ gets incremented and reaches Vo/2 whereas that of $\mathrm{S}_{7}$ falls to $\mathrm{Vo} / 2$ and $\mathrm{S}_{10}$ falls to zero. Although $\mathrm{S}_{9}$ is still on but then also the conduction by the body diode of $\mathrm{S}_{10}$ initiates. Finally, at $t_{6}$ when $i_{L}$ is negative the $S_{10}$ gets turned on with ZVS after which a linear increment could be observed in the current $\mathrm{i}_{\mathrm{L}}$ as per the relation mentioned in eqn. (13).

$$
\begin{gather*}
\left\{\begin{array}{c}
V_{12}=V_{c} \\
V_{34}=V_{o} \\
i_{L}(t)=i_{L}\left(t_{4}\right) \frac{V_{12}-V_{34} / n}{L}\left(t-t_{4}\right)
\end{array}\right\}  \tag{12}\\
\left\{\begin{array}{c}
V_{12}=V_{c} \\
V_{34}=V_{o} / 2 \\
i_{L}(t)=i_{L}\left(t_{6}\right) \frac{V_{12}-V_{34} / n}{L}\left(t-t_{6}\right)
\end{array}\right\} \tag{13}
\end{gather*}
$$

The duty cycle $d$ at the output side and phase shift ratio $\phi$ control the transferred power $P_{0}$ by the converter [32]. Different waveforms of $i_{L}$ for fixed input power and voltage are achieved by varying the possible combinations of $\phi \& d$ which further leads to different ZVS conditions. The waveforms showing the operation of this converter theoretically are represented in Figure 5. The switches are turned on during $\mathrm{t}_{1}-\mathrm{t}_{5}$. The value of current $i_{L}$ flowing through leakage inductance $L$ at these moments can determine the Zero Voltage Switching value. A piecewise relation exists between $P_{0}$ and $\phi$. For $V_{\text {in }}>30 \mathrm{~V}$, a non-monotonic relation is observed between $P_{0}$ and $\phi$ where a minimum point for $P_{0}$ exist. The coordinates thus can be given by:

$$
\begin{equation*}
\Phi=\frac{6 m^{2}-19 m+12}{2\left(9 m^{2}-36 m+40\right)} \tag{14}
\end{equation*}
$$

$$
\begin{equation*}
P_{o}=\frac{m T_{S} V_{i n}^{2}(m-1)(m-2)}{L\left(3 m^{2}-12 m+8\right)} \tag{15}
\end{equation*}
$$

The non-monotonicity causes instability which could be avoided if the minimum power is higher than the rated power. This could be accomplished if the value of leakage inductance satisfies the following relationship:

$$
\begin{equation*}
L<\frac{m T_{S} V_{\text {in }}^{2}(m-1)(m-2)}{P_{\text {rated }}\left(3 m^{2}-12 m+8\right)} \tag{16}
\end{equation*}
$$

The ZVS condition for switches at the primary side can be given by:

$$
\begin{equation*}
i_{L}\left(t_{o}\right)>i_{L 2}\left(t_{o}\right) \tag{17}
\end{equation*}
$$

The relation between input inductance and leakage inductance can be given by:

$$
\begin{equation*}
L_{i n}\left(-8 m^{2}+8 m d+m-2\right) L \tag{18}
\end{equation*}
$$

The range of $m, d, \phi$ can be concluded as:

$$
\left\{\begin{array}{c}
0 \ll 0.5  \tag{19}\\
0<d<0.5 \\
+d<0.5 \\
1.1<m<1.8
\end{array}\right\}
$$

In order to ensure ZVS, the design specification for input side inductance at the primary side is

$$
\begin{equation*}
L_{i n}<5 L \tag{20}
\end{equation*}
$$

The range of voltage ripple across $\mathrm{C}_{1}$ should be narrow. Thus, the clamping capacitor should be designed accordingly. The voltage across the clamping capacitor can be obtained by:

$$
V_{c}(t)=\left(\begin{array}{l}
t  \tag{21}\\
\int_{t_{o}} \\
\left(i_{L 1}\right. \\
\left.\left.(t)-i_{L}(t)\right) d t\right) / C_{1}+V_{o} .
\end{array}\right.
$$

$\Delta V_{c}$, voltage ripple across the capacitor $\mathrm{C}_{1}$ can be calculated by:

$$
\begin{equation*}
\Delta V_{c}=\max \left\{V_{c}\left(t_{x a}\right), V_{c}\left(t_{x c}\right)\right\}-\min \left\{V_{c}\left(t_{o}\right), V_{c}\left(t_{x \mathrm{~b}}\right)\right\} \tag{22}
\end{equation*}
$$

The current $i_{\mathrm{L} 1}$ intersects $\mathrm{i}_{\mathrm{L}}$ at three instants $t_{\mathrm{xa}}, t_{\mathrm{x} b}$, and $t_{\mathrm{xc}}$ as shown in Figure 5(b). The following conditions should be satisfied so as to limit $\Delta V_{c}$ to a smaller value.

$$
\begin{equation*}
\frac{\Delta V_{c}}{V_{c}}=\frac{\Delta V_{c}}{2 V_{i n}} 5 \% \tag{23}
\end{equation*}
$$

The duty cycle of the switches at the input side is fixed to 50 with an open loop control scheme thus the value of clamping capacitor $\mathrm{C}_{1}$ can be taken as $60 \mu \mathrm{~F}$. Thus, the average voltage across the clamping capacitor can be found out by:

(a)

(b)

Figure 5(a,b): Converter waveforms, Figure 5(a): Operating waveforms of the converter, Figure 5(b): Theoretical waveforms of the converter.

$$
\begin{equation*}
V_{c}=2 V_{i n} \tag{24}
\end{equation*}
$$

For identical input inductors $L_{1}$ and $L_{2}$, the input current $i_{i n}$ can be given as

$$
\begin{equation*}
i_{i n}(t)=i_{L 1}(t) i_{L 2}(t) \tag{25}
\end{equation*}
$$

Thus, it is evident that if $L_{1}$ and $L_{2}$ are identical then there will be zero high-frequency current ripple and $i_{i n}$ will be a constant DC current. The low-frequency ripple is also suppressed in this converter by using a dual-loop control. This increases the impedance at the output of the converter which reduces the current ripple obtained from the stacked fuel cell.

## Four-phase interleaved four-switch buck-boost converter

Interleaving technology improves the converter's dynamic response and power density making it more widely used for high-power applications [34]. This interleaved DC/DC converter is multi-phased and employs magnetic integration which reduces the converter's cost as well as enhances the power density $[35,36]$. The phases interleaved strategy reduces the ripple present at the output of the converter [37]. A fourmode control strategy is proposed in [38] to improve the converter's control strategy. For reduction in inductor current ripple, the Zero Voltage Strategy of this converter should be realised at its full range [39,40]. The schematic diagram of a

Four-Phase Interleaved Four-Switch Buck-Boost Converter is shown in Figure 6. Here in Figure $6 \mathrm{~L}_{1---4}$ represents inductance \& $M$ describes the switches. The converter consists of four switches $\mathrm{S}_{1}, \mathrm{~S}_{2}, \mathrm{~S}_{3}$ and $\mathrm{S}_{4}$ along with an output filter capacitor $C_{0}$ and a shared inductor L. Here, the switches $S_{1}$ and $S_{2}$ form a buck bridge whereas $\mathrm{S}_{3}$ and $\mathrm{S}_{4}$ form a boost bridge both with complimentary conduction [41]. The duty cycle of switch $\mathrm{S}_{1}$ and switch $S_{3}$ is denoted by $d_{1}$ and $d_{2}$ respectively. The converter's voltage gain $M$ can be achieved using the principle of voltsecond balance after non-ideal parameters are ignored these parameters are parasitic components of the circuit and power loss.

$$
\begin{equation*}
M=\frac{V_{o}}{V_{\text {in }}} \frac{d_{1}}{1-d_{2}} \tag{26}
\end{equation*}
$$

It can be said that $M$ is affected only due to $d_{1}$ and $d_{2}$ whereas the gain of the converter is not affected due to the phase shift angle between two bridge arms and switching frequency. The interleaving technology is provided through magnetic integration which consists of inductors. This interleaving technology is useful to reduce large ripples in input and output current, and high current stress of the switches, and improves the converter's overall efficiency. There is a phase difference of $90^{\circ}$ between every two phases as it drives the corresponding switch. There is no decrement in the ripples in the inductor current of each phase thus increasing the number of interleaving phases which further increases the weight and volume of the magnetic element. The significant integration of magnetic circuits to interleaved circuits improves the dynamic performance as well as reduces the losses of magnetic elements of the converter. Figure 7 shows the topology of the four switch, Four-Switch Buck-Boost Converter.

The converter here operates in a three-mode control strategy as per the input and output voltage relation where the three modes are boost, buck, and buck-boost. If the value of $d_{1}$ of Buck Bridge is 1 , at this instant $S_{1}$ is on, $S_{2}$ is off and the switching actions are performed by $\mathrm{S}_{3}$ and $\mathrm{S}_{4}$ then the converter behaves like a synchronous rectifier boost converter. If the value of $d_{2}$ of Boost Bridge is 0 , at this instant $S_{4}$ is on, $S_{3}$ is off and the switching actions are performed by $S_{1}$ and $S_{2}$ then the converter behaves like a synchronous rectifier Buck converter. The moment when the value of output voltage $\mathrm{V}_{\mathrm{o}}$ is close to input voltage then all four switches will turn on at the same time and the converter will operate in buck-boost mode. At a time, two switches are turned on whereas switches forming


Figure 6: A schematic representation of Four-Phase Interleaved Four-Switch BuckBoost Converter topology [23].
the corresponding bridge arms are also turned on at a phase shift of $90^{\circ}$ for preventing the direct voltage. Table 1 shows all the switching states of the converter operation. Here, $\mathrm{V}_{\mathrm{ab}}$ represents the inductor voltage.

The equivalent circuit of all operating modes of the converter is shown in Figure 7(a-d). In mode 1 shown in Figure 7(a), the load receives the stored energy released by the inductor in boost mode. This same could happen in buck mode also where energy storage by the inductor is made possible using the battery. Mode 2 occurs in boost mode as shown in Figure 7(b). To realize higher output voltage in comparison to input voltage the inductor uses more energy to charge. Mode 3 occurs in buck mode where the inductor releases stored energy as

Table 1: Switching states of FSSB converter.

| Operating modes | $\mathbf{S}_{1}$ | $\mathbf{S}_{2}$ | $\mathbf{S}_{3}$ | $\mathbf{S}_{4}$ | $\mathbf{V}_{\text {ab }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 0 | 1 | $\mathrm{~V}_{\text {in }}$-Vo |
| 2 | 1 | 0 | 1 | 0 | $\mathrm{~V}_{\text {in }}$ |
| 3 | 0 | 1 | 0 | 1 | $-\mathrm{V}_{0}$ |
| 4 | 0 | 1 | 1 | 0 | 0 |

shown in Figure7(c). This mode doesn't appear in boost mode but can appear in the Buck-Boost mode as there is a circulation of inductor current. Practically, for control purposes the time for the circulation current of the inductor should be less. The main waveforms of inductor current and voltage and driving voltage of three operating modes are shown in Figure 7(d). The waveform of the driving voltage, inductor current, and inductor voltage of the converter under three mode control for three operating modes is shown in Figure 8. There is a frequent transition of the modes in this transistor due to disturbances which could be reduced by adding $\Delta$. The waveforms of the ripple of the inductor current and output current of each phase of a four-phase interleaved FSBB converter are shown in Figure 9. It is observed that after a phase interleaved connection there is an offset in the ripple current of the inductor.

Table 2 below shows a comparison of the Clamped H-type boost DC-DC converter, Current-Fed Hybrid Dual Active Bridge DC-DC Converter, and Four-Phase Interleaved Four-Switch Buck-Boost Converter based on parameters like Voltage Gain, switching components, diodes, etc. The table shows that each capacitor has different properties and can be used as per the functional requirement, and disturbances on load.


Figure 7: Topology of Four-Switch Buck-Boost Converter. The schematic representation of different configurations of the converter at different modes is shown in Figure $7(\mathrm{a}-\mathrm{d})$.



Figure 7(b): Mode 2.


Figure 7(d): Mode 4.

## Conclusion

There are several isolated and non-isolated converters available in the market. The non-isolated converters are simple, efficient, and easy to maintain which makes them popular in comparison to others. This paper dealt with three such nonisolated converter configurations that are popular and have been used widely in recent times for vehicular applications. These three converters are a clamped H-type boost DC-DC converter, a current-fed hybrid DAB DC-DC converter, and a four-phase interleaved four-switch Buck-Boost converter. The performance of converters is analysed on the basis of voltage
gain, size of the circuit, efficiency, and voltage stress. As seen in the study, the capacitor-clamped H-type boost DC-DC converter has several benefits wide voltage gain range while ignoring the narrow-pulse of PWM voltage waveform, lower power conduction loss of switches, lower voltage stress on capacitors and power semiconductors and lower input current ripple. Similarly, a current-fed hybrid DAB DC-DC converter has less high-frequency ripples of input current in comparison to conventional interleaving technology. The notch filter as seen here effectively reduces the low frequency. Finally, a four-phase interleaved four-switch Buck-Boost converter topology reduces ripples of output current to a large extent


Figure 8: Three-mode control waveforms of converter: (i) Boost (ii) Buck-Boost (iii) Buck.


Figure 9: Waveforms of the output current ripple \& inductor current ripple of each phase.

Table 2: Comparison of the above three mentioned converters.
$\begin{array}{|c|c|c|c|c|}\hline \text { S. } \\ \text { No. }\end{array}$ Parameters $\left.\begin{array}{c}\text { Clamped H-type } \\ \text { boost DC-DC } \\ \text { converter }\end{array} \begin{array}{c}\text { Current-Fed Hybrid } \\ \text { Dual Active Bridge DC- } \\ \text { DC Converter }\end{array} \quad \begin{array}{c}\text { Four-Phase } \\ \text { Interleaved Four- } \\ \text { Switch Buck- } \\ \text { Boost Converter }\end{array}\right]$
and improves the efficiency. This converter has three modes of operation depending on the input-output voltage relationship. They are Buck, Buck-Boost, and Boost modes. This three-mode control strategy solves the discontinuous voltage gain issue and shows good dynamic performance while maintaining a smooth transition between these three modes. Although they can be applied in various fields, they are most suitable for vehicular and power generation applications specifically for fuel cell stacks.

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